

Application No. 09/558,542

**REMARKS**

Claims 1-20 are pending in this application. By this Amendment, claims 1 and 11 are amended. Reconsideration based on the foregoing amendments and following remarks is respectfully solicited.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (e) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection. Entry of the amendments is thus respectfully requested.

The Office Action rejects claims 1-20 under 35 U.S.C. §102(b) over Benson (U.S. Patent 5,301,325). This rejection is respectfully traversed.

Applicants respectfully submit that Benson does not disclose, "a controller, the controller dividing the source code into code blocks based on the target processor register capability." Support for the claim amendments may be found, for example, on page 4, lines 5-7 of the specification.

Instead, Benson discloses in col. 10, lines 25-29, "A block of code is defined to be a sequence of tuples with no entry or exit between the first and last tuple. Usually a block starts with a label or routine entry and ends with a branch to another label." Therefore, Benson divides the source code into code blocks based on occurrence of branches and loops in the code.

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Nowhere in Benson is the target processor register capability considered when dividing the source code into code blocks. In fact, according to col. 9, lines 8-12, "In general, the front end converter 20 need not consider the architecture of the target machine 25 upon which the object code 23 will be executed, when the front end 20 is translating from source code 15". Therefore, Benson expressly does not consider the architecture of the target machine when translating from the source code, and actually teaches away from the present invention.

While Benson does "track register usage to determine which registers are destroyed by a routine, and generate routine prologue and epilogue code which perform 64-bit register saves," nowhere in Benson is it disclosed that this information is used to divide the source code.

Therefore, the subject matter recited in claim 1 is not anticipated by Benson. Therefore, Applicants respectfully request that the rejection of independent claim 1 and dependent claims 2-10 be withdrawn.

The Office Action rejects claims 11-20 under 35 U.S.C. §102(b) over Benson. However, claim 11 recites the same patentable feature as was recited in claim 1, which is "dividing the source code into blocks based on the target processor register capability." Therefore, claim 11 recites patentable subject matter for similar reasons as set forth above. Applicants respectfully request the rejection of independent claim 11 and dependent claims 12-20 be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

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Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

**PROPOSED**

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